never accessed at the same time, access transistors can also be configured to couple the upper memory cell 120 to column line A. The use of a separate column line B for the upper memory cell 120, however, would enable both cells to be accessed at the same time to simultaneously store and retrieve two bits of data. In such a case the grid decoder can be omitted.

IN THE CLAIMS:

Please amend the claims as follows.

17. (Amended) A method of fabricating a memory device comprising:

forming a first memory cell to include a chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material;

forming a second memory cell to include a chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material;

forming a common anode for both of said first and second memory cells, wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer.

19. A method as in claim 17 further comprising:

forming each of said first and second memory cells of a layered structure which includes a cathode layer, a chalcogenide glass material layer having a changeable resistance and a anode layer.

21. (cancel without disclaimer or prejudice)

22. A method as in claim 17, wherein said middle conductive layer comprises tungsten.

23. (Amended) A method as in claim 18 further comprising:

forming said stacked first and second memory cells over a conductive plug such that said cathode of said second memory cell is in electrically coupled with said conductive plug.

24. (Amended) A method as in claim 23 further comprising a column line conductor electrically coupled to a second active region of a first access transistor.

25. (Amended) A method as in claim 23 further comprising forming a word line conductor which is electrically coupled to a gate of a first access transistor.

26. (Amended) A method as in claim 23 further comprising forming a second access transistor and electrically coupling said second access transistor to said second memory cell.

27. (Amended) A method as in claim 26 wherein said first and second memory cells are coupled to different column lines by said first and second access transistors.

28. (Amended) A method as in claim 17 wherein said first and second memory cells are connected to the same column line by said first and second access transistors.

29. (Amended) A method as in claim 26 further comprising:

Cancld B4

forming a circuit for operating said first and second access transistors separately to individually access each of said first and second memory cells.